A HIGH FIGURE OF MERIT AND AREA-EFFICIENT LOW-VOLTAGE (0.7-1 V) 12 GHz CMOS VCO

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Abstract - **This paper presents the design and experimental results of an area-efficient LC-based voltage controlled oscillator (VCO) which can operate from a supply voltage as low as 0.7 V (2 mW in power), while being suitable for RF applications. A transformer coupling technique is used to reduce the required silicon area by more than a factor of two, compared to earlier designs, while reducing the phase noise. A VCO occupying a 0.24 mm^2 of area was fabricated in a standard 0.18 μm CMOS process. With a 1 V supply, the 12 GHz VCO consumes 7.7 mW with a measured phase noise of -102.2 dBc/Hz at a 600 kHz offset. A tuning range of 400 MHz is achieved without using varactors. The VCO has an excellent figure of merit (FOM) of -183.4 dBc/Hz, compared to recent designs [1].**

I. INTRODUCTION

Driven by the insatiable demand for lower cost, wider bandwidth, and higher data rates in both wireless and optical systems, integrated circuit (IC) designs are constantly evolving towards denser integration and higher frequencies (i.e. in the GHz range). In particular, the quest for single-chip solutions for transceivers has resulted in a remarkable growth of interest in CMOS RFIC designs (e.g. [1]-[11]). Furthermore, attributed to the continuous devices down scaling and the need to reduce the power consumption of the digital circuitry, the supply voltage standards for integrated circuits continue to decrease towards sub-1 V. This trend has motivated the evolution of low-voltage RFIC design topologies (e.g. [3]-[5], [10]-[11]).

The voltage controlled oscillator is one of the key building blocks in RF transceivers. A number of performance requirements have to be met in order to make a VCO suitable for wireless applications. Most importantly, low phase-noise is required to avoid corrupting the mixer-converted signal with closeby interfering tones. In addition, low power consumption and adequate frequency tuning are also two important aspects that define the performance of a VCO. Compact VCO designs which occupy small silicon real estate are always desirable, as area-efficient designs directly translate into reduction in cost.

This paper proposes the use of a transformer coupling technique to considerably reduce the size of a low-voltage LC-based VCO architecture [4], while considerably reducing its phase noise through the enhancement of the quality factor of the LC-tank. A 12 GHz VCO prototype was implemented in a standard 0.18 μm CMOS process to verify the approach proposed. It can operate from a supply voltage as low as 0.7 V resulting in very low power consumption (2 mW), while maintaining a low phase noise and a reasonable tuning range.

The following section introduces the low-voltage VCO topology, which is based on the conventional complementary cross-coupled LC architecture, with modifications to allow for sub-1 V operation. Detailed design equations and circuitry are discussed in Section 3. Techniques to realize an area-efficient low phase noise implementation are presented in Section 4. Finally, the paper concludes with experimental results and a comparison to other CMOS VCO circuits recently reported.

II. LC-BASED VCO TOPOLOGIES

With the targeted voltage supply down to 1 V, there is a limited number of VCO topologies suitable for high frequency operation. The NMOS only cross-coupled structure can operate at sub-1 V, but suffers from poor phase noise at high frequencies, which becomes limited by the Q-factors of the tuning varactors (e.g. [2], [5]). The PMOS only cross-coupled structure has better phase noise, but often requires high power consumption, due to the intrinsic low transconductance (g_m) of the PMOS transistors [7]. The complementary cross-coupled structure (Fig. 1(a)) features a good balance between low phase noise and low power consumption, but requires a high supply voltage (i.e. 2-3 V) due to transistor stacking, which makes it not suitable for low-voltage applications. The low-voltage VCO topology used in this paper is a variation of the conventional complementary cross-coupled structure.

A. THE COMPLEMENTARY DIFFERENTIAL LC-STRUCTURE

Many recent publications have shown that the complementary cross-coupled structure in Fig. 1(a) is suitable for very high frequencies of oscillation (e.g. [3], [6]). This structure uses both NMOS (M_1-M_2) and PMOS (M_3-M_4) cross-coupled amplifiers to provide the negative resistance necessary to compensate for the losses in the differentially excited inductor L. The resonant tank consists of the parasitic capacitances of transistors (M_1-M_4) and of the inductor. Frequency tuning is achieved by controlling the back-gate voltages of the PMOS transistors, thus eliminating the use of varactors. There are several desirable features to this topology:

1) The effective quality factor of the resonant tank is increased, as the inductor is differentially excited. This results in a decrease in phase noise.
2) Varactors, which tend to degrade the tank quality factor at high frequencies, are eliminated. This also allows for higher frequency of oscillation.
3) The resonant tank is formed in a loop configuration without any ground referencing (details in Section 3, Fig. 2(b)). Hence, the frequency of oscillation is less sensitive to component parasitics to the substrate.

The main drawback of this topology is the need for a relatively high supply voltage (i.e. 2-3 V) [3], as it requires at least two transistor stacks between the supply rails. Also, the maximum frequency tuning range achieved by only controlling the back-gate voltages of the PMOS transistors is limited.

B. LOW-VOLTAGE COMPLEMENTARY LC-STRUCTURE

The evolution towards a low-voltage complementary differential LC-structure is shown in Fig. 1. To overcome the high supply voltage requirement of the conventional structure in Fig. 1(a), capacitors (C) are added between the cross-coupled

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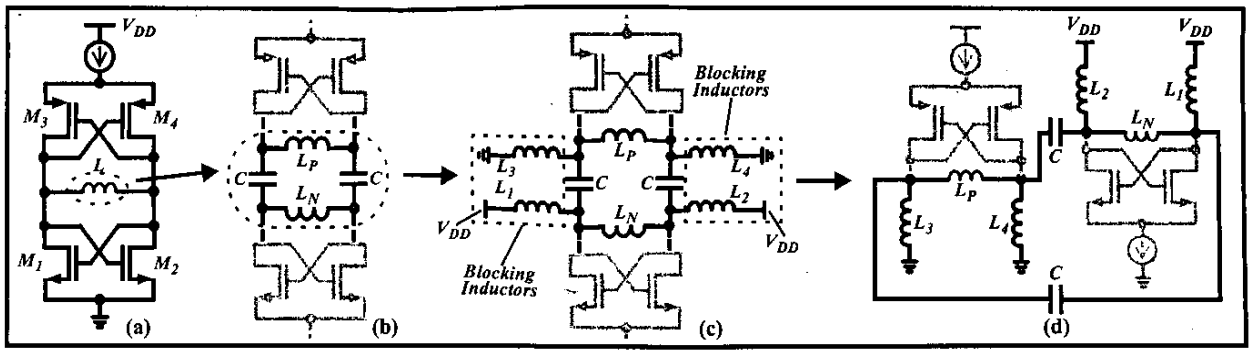

Fig. 1: Evolution of the complementary differential LC-structure toward a low-voltage realization.

PMOS and NMOS amplifiers. This is to decouple the DC bias without affecting the AC signal paths. The capacitors can be viewed as short circuits at very high frequencies. To preserve symmetry, the tank inductor (L) is decomposed into two inductors ($L_{N,P}$) connected in parallel, as shown in Fig. 1(b). Blocking inductors (L_1-L_4) are added to provide a DC path for the two cross-coupled pairs, while presenting a high impedance to the AC signals (Fig. 1(c)).

The resulting topology shown in Fig. 1(d) can operate from a very low voltage supply, while preserving the characteristics of the original complimentary structure discussed in Section 2. Furthermore, the frequency tuning of this structure is not only limited to controlling the back-gate voltages of the PMOS tank, but can also be extended by simultaneously varying the bias current of the PMOS amplifiers. This is now possible since the DC currents between the two cross-coupled pairs have been decoupled. This results in a wider tuning range as will be shown later (Fig. 6).

III. Design Issues and Equations

A detailed schematic of the low-voltage VCO is shown in Fig. 2(a). The LC resonant tank in this circuit is composed of the two differential inductors ($L_{N,P}$) in parallel with the total capacitance seen at the oscillation nodes, namely the parasitic capacitances of the inductors, and the drain-gate (C_{dg}) and gate-source (C_{gs}) capacitances of transistors (M_1-M_4). The AC equivalent circuit of the resonant tank is shown in Fig. 2(b). Note that the tank components form a closed-loop, making the circuit's frequency of operation less sensitive to the component parasitics to the substrate.

The oscillation frequency (f_o) is given by

$$f_o = \frac{1}{2 \cdot \pi \cdot \sqrt{L_{tank} \cdot C_{tank}}}, \quad (1)$$

where

$$L_{tank} = L_P \| L_N, \quad (2)$$

and

$$C_{tank} = C_{dg1} + C_{dg2} + C_{gs1} \| C_{gs2} + C_{dg3} + C_{dg4} + C_{dg3} \| C_{dg4}. \quad (3)$$

The resonator of an LC oscillator cannot maintain steady oscillation by itself, due to the energy lost per cycle through the parasitic resistances of the tank. For a narrowband of frequencies, all the parasitic resistances in an LC tank can be modeled by a single parallel resistance (R_{tank}). In most cases, the inductors exhibit the lowest quality factors, hence their series resistances (R_L) will dominate the tank's resistance. By applying series-shunt transformation, the equivalent parallel resistance (R_{tank}) of the tank can be shown to be

$$R_{tank} \approx (Q_{tank}^2 R_{L_N}) \| (Q_{tank}^2 R_{L_P}) \approx Q_{tank}^2 \frac{R_L}{2}, \text{(for } R_{L_N} = R_{L_P}) \quad (4)$$

where $R_{L(N,P)}$ are the series resistances of inductors ($L_{N,P}$) in Fig. 2(b), and Q_{tank} is the quality factor of the resonant tank [3].

In order to compensate for the energy loss and sustain oscillation, two cross-coupled amplifiers are used in this topology to provide the negative resistance, i.e. $-R = 2/(g_{m12} + g_{m34})$, where $g_{m12,34}$ are the transconductances of the cross-coupled M_1-M_2 and M_3-M_4 pairs respectively. To ensure oscillation startup, the total transconductance (G_m) must be chosen to satisfy

$$G_m = g_{m12} + g_{m34} \geq \frac{2}{R_{tank}} = \frac{2}{Q_{tank}^2 (R_L/2)} = \frac{4}{Q_{tank}^2 R_L}. \quad (5)$$

IV. Area-Efficient Design and Layout Techniques

As silicon area translates directly to cost, compact designs are always desirable, provided that signal integrity and performance are not compromised. Clearly, the design in Fig. 2(a) is suitable for low-voltage operation, but this comes at the expense of an increasing number of passive components. In particular, this topology requires two differentially excited inductors, four AC-blocking inductors, and two coupling capacitors, as opposed to the only one inductor required in the original topology (Fig. 1(a)). Area-efficient design and layout techniques are therefore needed.

A. AC-Blocking Inductors (L_{BLK})

Inductors L_1-L_4 serve two functions in this topology: i) they provide a DC path for the resonant tank, and ii) they act as AC-blocking impedances, in order to prevent AC signal losses to the power supplies. To achieve good signal blocking, the impedance of each AC-blocking inductors (Z_{Lblk}) must be much greater than the impedance of the tank (Z_{tank})

$$Z_{Lblk} = j\omega_o L_{blk} \gg Z_{tank}. \quad (6)$$

Since the required inductance for signal blocking is large, and an accurate value is not critical, bonding and package lead inductances can be used. This is very practical since the DC biasing of the resonant tanks are either connected to V_{DD} or to ground, and both will anyway need to be connected to off-chip power supplies. A blocking inductance of 5 nH can easily be achieved.

B. Differential Transformer-Like Coupled Tank

An on-chip tank inductor in a typical VCO can consume more than 50% of the chip area, due to it's inherently large physical size

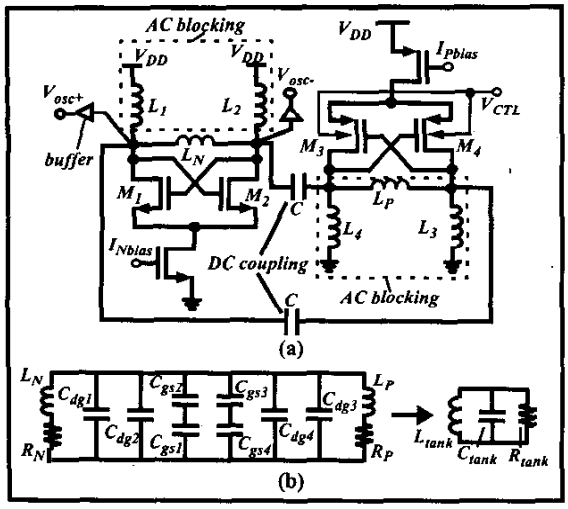

Fig. 2: (a) Schematic of the low-voltage complementary VCO, and (b) AC equivalent circuit of the resonant tank.

(e.g. [1], [4]). In this design, the tank has two integrated inductors ($L_{N,P}$) connected in parallel, compared to only one inductor in the original topology†. This results in a substantial increase in area. To mitigate this, the two inductors are intertwined to minimize area, and laid out very close to each other (Fig. 3). Their AC currents are flowing in the same direction, in order to benefit from the transformer-like mutual inductance, thus improving the quality factor and reducing the phase noise. The total tank inductance is now the combination of the self- and mutual-inductances of L_N and L_P, and can be approximated by

$$L_{tank} = L_{self} + 2L_{mutal} = (L_N + M) \| (L_P + M), \quad (7)$$

where $M = k\sqrt{L_N L_P}$, and $k \approx 0.7$ is the coupling factor between L_N and L_P.

In this work, the initial tank inductance value was calculated based on the above equation. Then, a more accurate value was obtained using a commercially available EM simulator (Agilent ADS). The estimated tank inductance is 0.4 nH, with a quality factor Q = 9 at 12 GHz††.

C. Coupling Capacitors

Coupling capacitors (C) are used to decouple the DC bias and allow for low-voltage operation. Their sizes need to be chosen to ensure they present low impedance paths to the RF signals between the NMOS and PMOS pairs. The following condition must be satisfied

$$2C \gg C_{tank}, \quad (8)$$

where C_{tank} is the total capacitance of the resonant tank.

In this design, high quality metal-insulator-metal (MIM) capacitors with a density of 0.9 fF/μm^2 were used. To accommodate for the layout orientation of the inductors, coupling capacitors are used to bridge the tank inductors from two ends (i.e. between V_{P+}, V_{N+} and V_{P-}, V_{N-}) as shown in Fig. 3. This results in a compact and area-efficient design of the entire resonant tank. The size of the coupling capacitance used is 11.7 pF.

† Note that only one inductor of value ($L_{N,P}/2$) could be used. This however will limit the minimum inductance value that could be achieved, thus imposing an upper limit on the maximum oscillating frequency. Also, it will not be possible to benefit from the transformer-like coupling between the two inductors which, as shown here, can improve the quality factor of the inductor by almost a factor of two.

†† This is considered to be a very good Q-factor for a low resistivity substrate CMOS process.

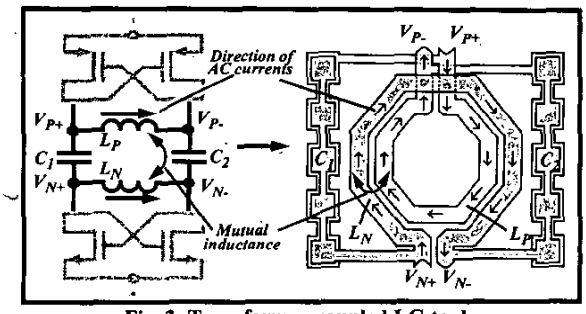

Fig. 3: Transformer-coupled LC-tank.

V. Measurement Results

The micrograph of the VCO is shown in Fig. 4. Symmetry is preserved throughout the entire layout. All DC and control signals are bondwired to the package, while standard ground-signal-ground pads are used for on-chip probing the RF output. The layout was done according to RF design guidelines, keeping DC traces thin and AC connections wide and as short as possible. The chip area is 0.24 mm^2, which is quite small when compared to other designs (e.g. 0.67 mm^2 in [1] or 0.93 mm^2 in [4]).

With a supply voltage of 1 V, the VCO consumes 7.7 mW with a measured phase noise of -102.2 dBc/Hz at a 600 kHz offset. It remains operational for a supply voltage as low as 0.7 V with a power consumption of 2 mW, as shown in Fig. 5.

Frequency tuning can be achieved through two mechanisms: i) by controlling the back-gate voltages of the PMOS tank (Fig. 6(a)), and ii) by varying the bias current supplied to the PMOS tank (Fig. 6(b)). Combining these two mechanisms results in a wider tuning range, as denoted by the diamond points in Fig. 6(a). A maximum tuning range of 400 MHz is measured.

To evaluate the overall performance of the VCO, a common figure of merit (FOM) is used, which is given by

$$FOM = L\{f_{offset}\} - 20\log\left(\frac{f_o}{f_{offset}}\right) + 10\log\left(\frac{P_{DC}}{1\,mW}\right), \quad (9)$$

where $L\{f_{offset}\}$ is the phase noise at a certain frequency offset (f_{offset}), f_o is the oscillation frequency, and P_{DC} is the power dissipation. With a supply voltage of 1 V and 0.7 V, this VCO has a FOM of -180.8 dBc/Hz and -183.4 dBc/Hz respectively. This compares well, if not exceeds, the specifications of recently published CMOS VCO's, while operating at lower voltage (0.7-1 V) as shown in Fig. 7. Table I summarizes the VCO performance.

VI. Conclusion

We have presented the design and experimental results of an area-efficient VCO which can operate from a supply voltage as low as 0.7 V (2 mW in power). A transformer-like resonant tank is used to reduce the required area, while improving the tank quality factor and reducing the phase noise. The 0.7 V VCO has an excellent FOM of -183.4 dBc/Hz, compared to recent work.

VII. ACKNOWLEDGMENT

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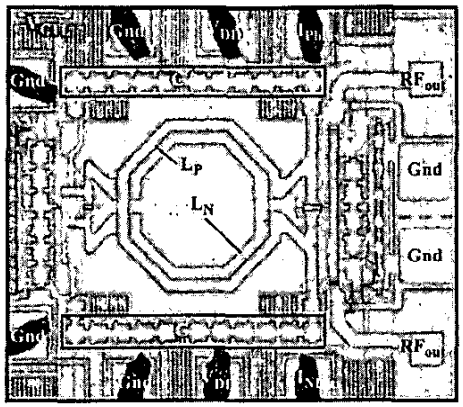

Fig. 4: Micrograph of the 12 GHz VCO.

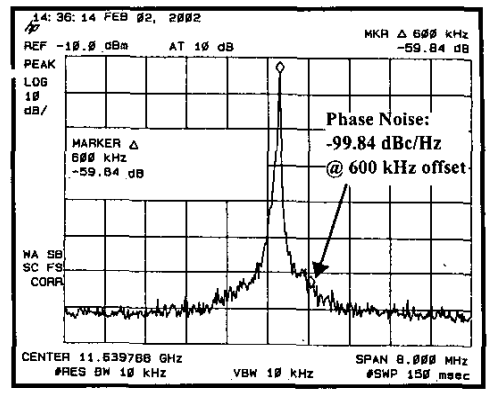

Fig. 5: Measured output spectrum of the 12 GHz VCO (V_{DD}=0.7 V), showing a phase noise of -99.84 dBc/Hz at a 600 kHz offset.

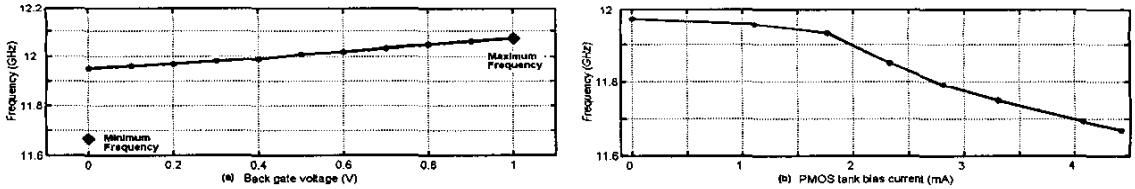

Fig. 6: Two frequency tuning mechanisms of the VCO through: (a) the PMOS back-gate voltages, and (b) the PMOS tank bias current. The two diamond points in Fig. 6(a) denote the minimum and maximum achievable frequencies, when both tuning schemes are combined.

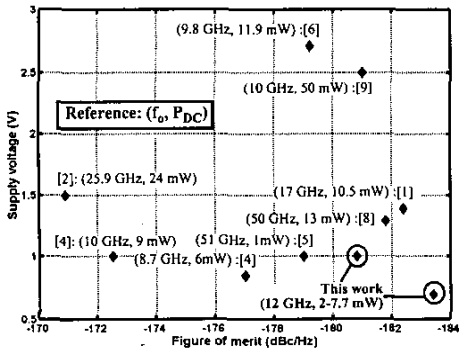

Fig. 7: Performance comparison to recently published CMOS VCO's, operating in the 8.7-51 GHz range.

	12 GHz VCO	
Technology	CMOS 0.18 µm	
Supply voltage	1 V	0.7 V
Power consumption	7.7 mW	2 mW
Phase noise @ 100 kHz offset	-88.1 dBc/Hz	-84.8 dBc/Hz
Phase noise @ 600 kHz offset	-102.2 dBc/Hz	-99.8 dBc/Hz
Phase noise @ 1 MHz offset	-106.4 dBc/Hz	-103.4 dBc/Hz
Tuning range	400 MHz	400 MHz
Chip area	0.24 mm^2	
Figure of merit @ 100 kHz offset	-180.8 dBc/Hz	-183.4 dBc/Hz

Table 1: Performance summary of the VCO.